FIG. 1 (PRIOR ART)

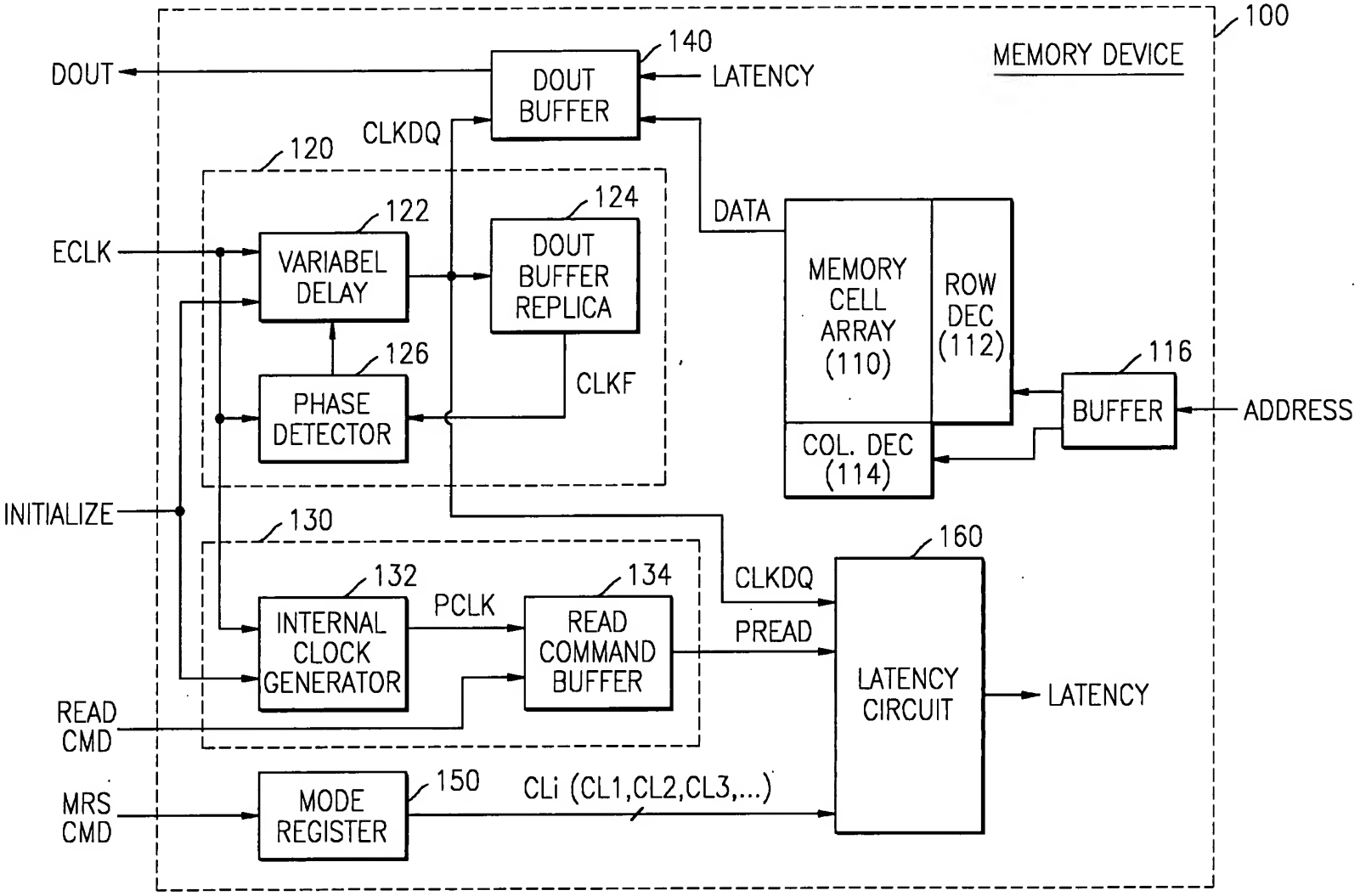


FIG. 2 (PRIOR ART)

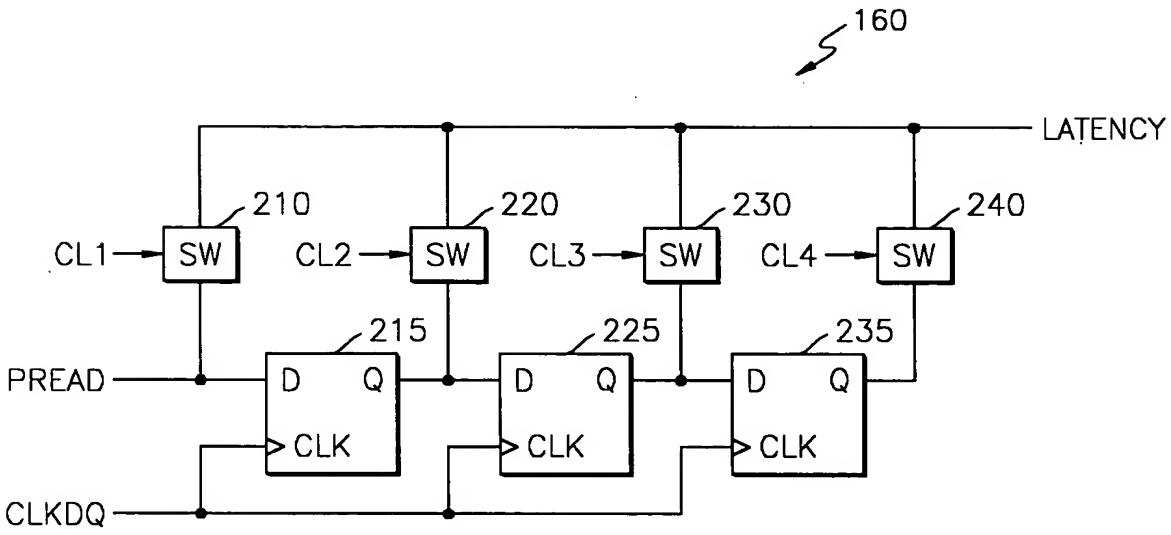


FIG. 3A (PRIOR ART)

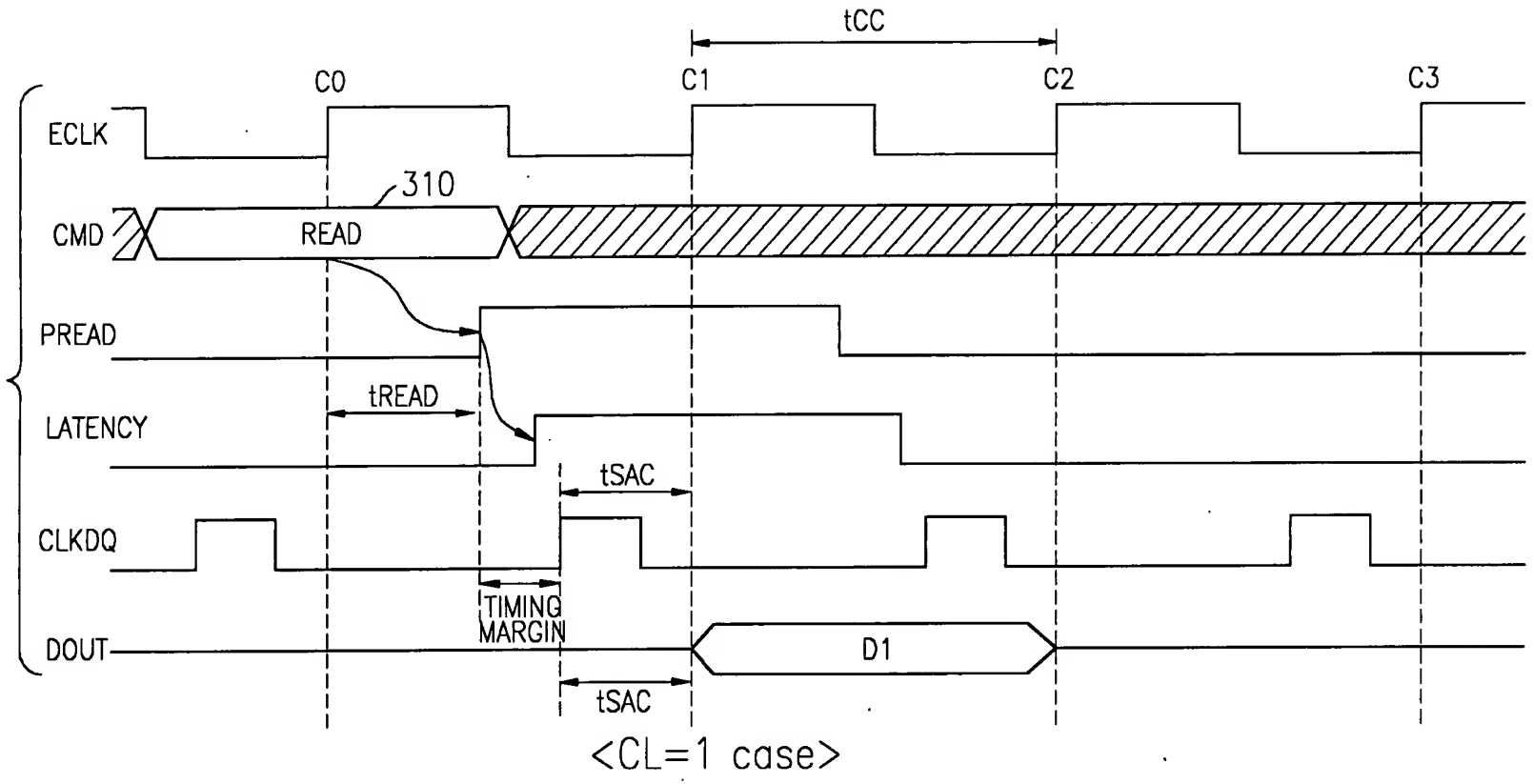


FIG. 3B (PRIOR ART)

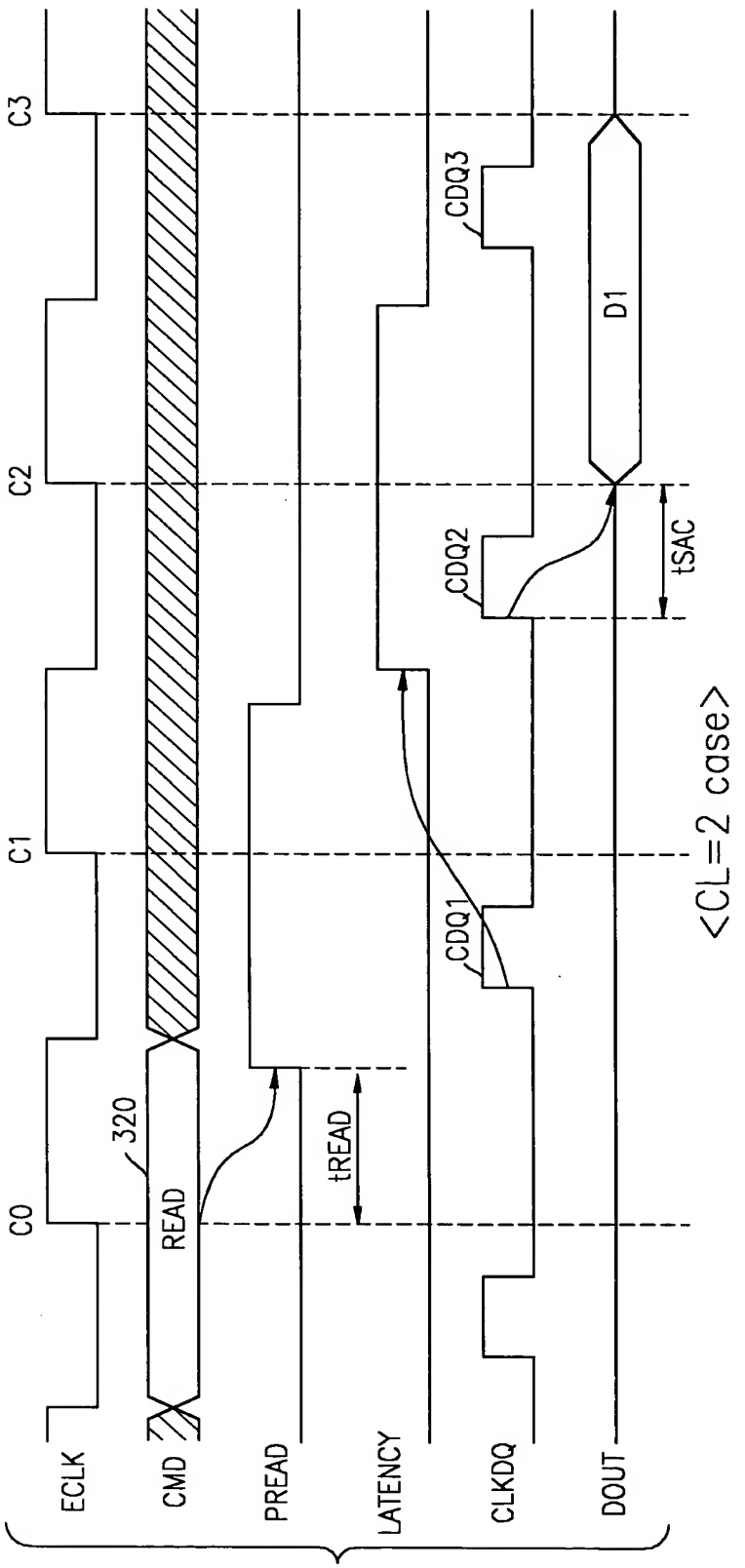
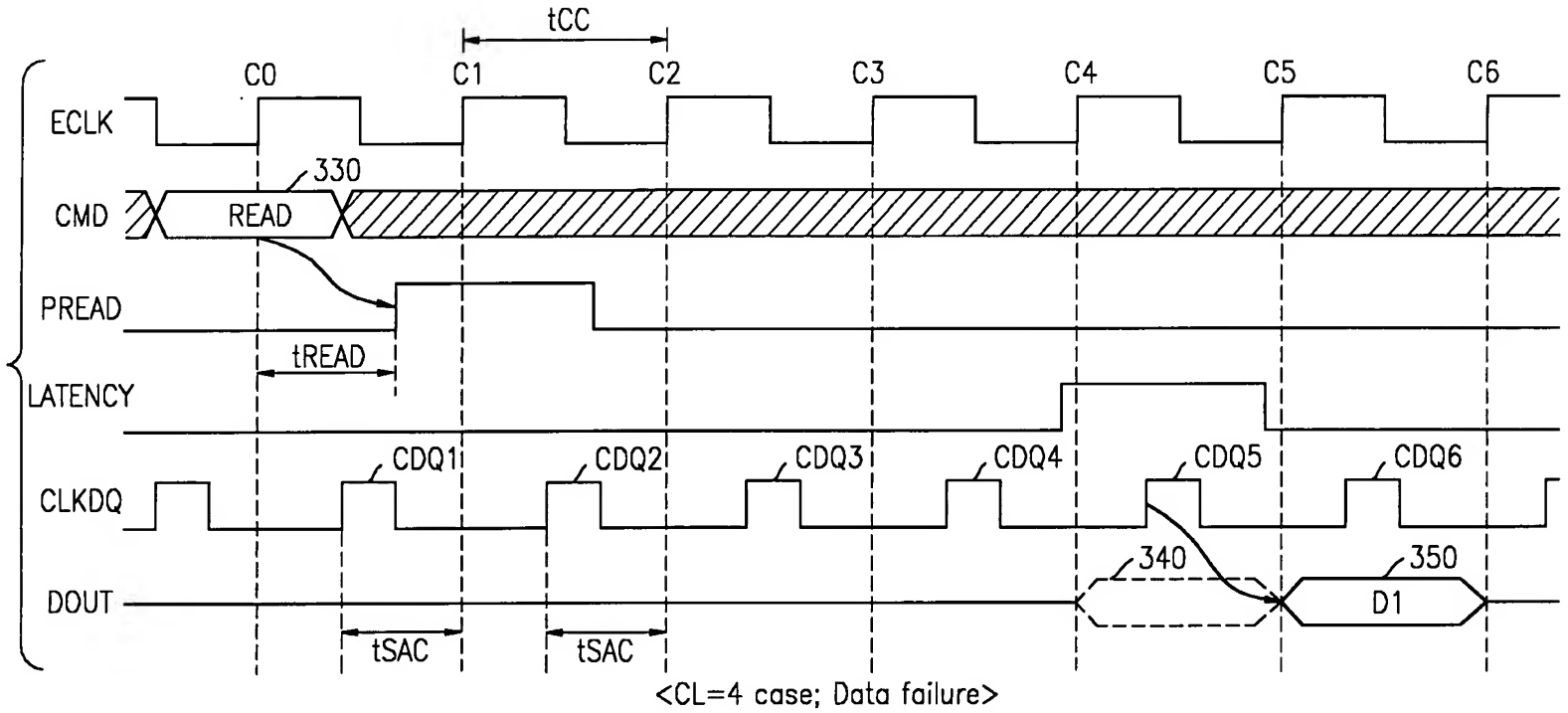


FIG. 3C (PRIOR ART)



<CL=4 case; Data failure>

FIG. 4A

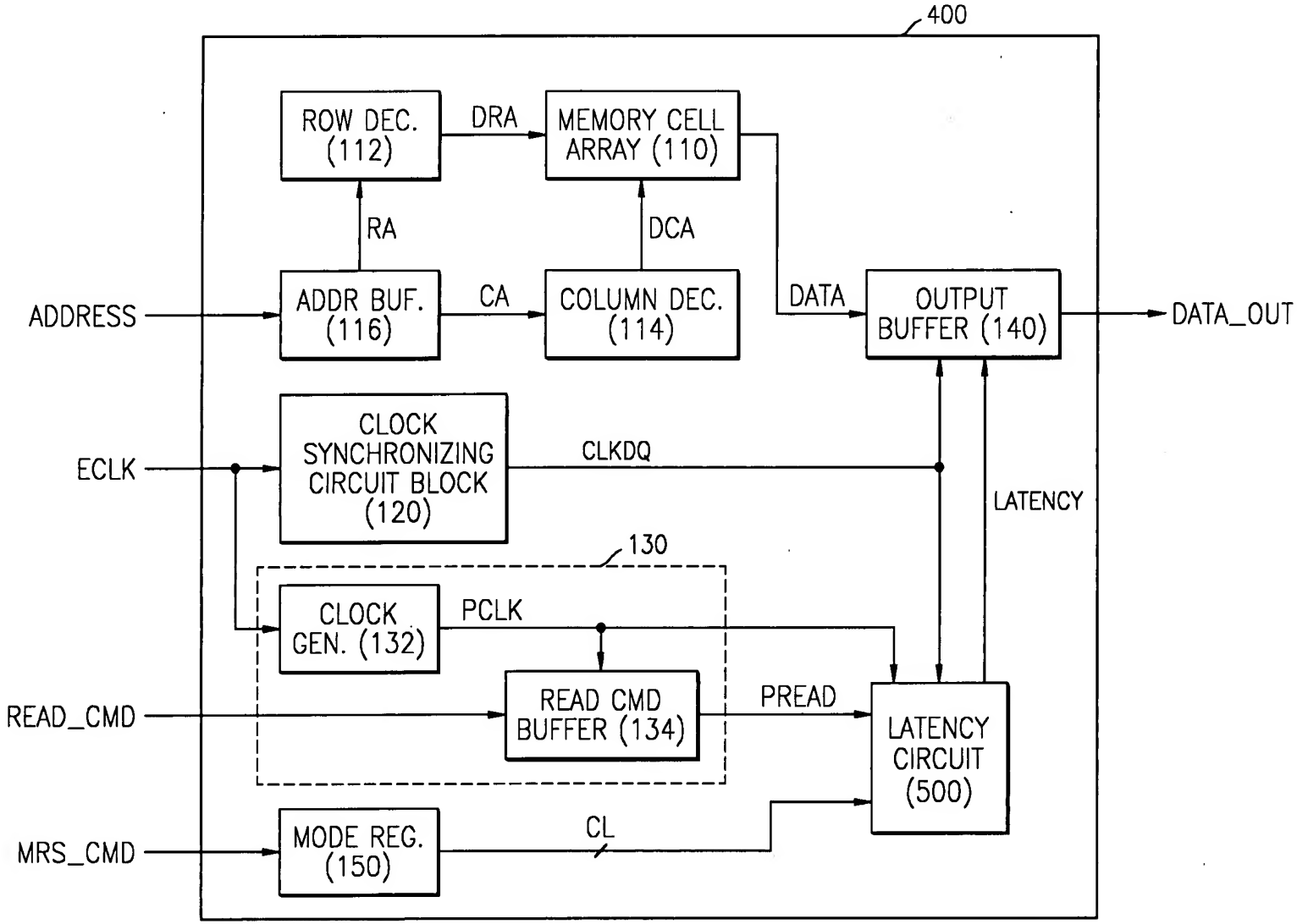

400
ROW DEC. (112)
DRA
MEMORY CELL ARRAY (110)
RA
DCA
ADDRESS
ADDR BUF. (116)
CA
COLUMN DEC. (114)
DATA
OUTPUT BUFFER (140)
DATA_OUT
ECLK
CLOCK SYNCHRONIZING CIRCUIT BLOCK (120)
CLKDQ
LATENCY
130
CLOCK GEN. (132)
PCLK
READ_CMD
READ CMD BUFFER (134)
PREAD
LATENCY CIRCUIT (500)
MRS_CMD
MODE REG. (150)
CL

FIG. 4B

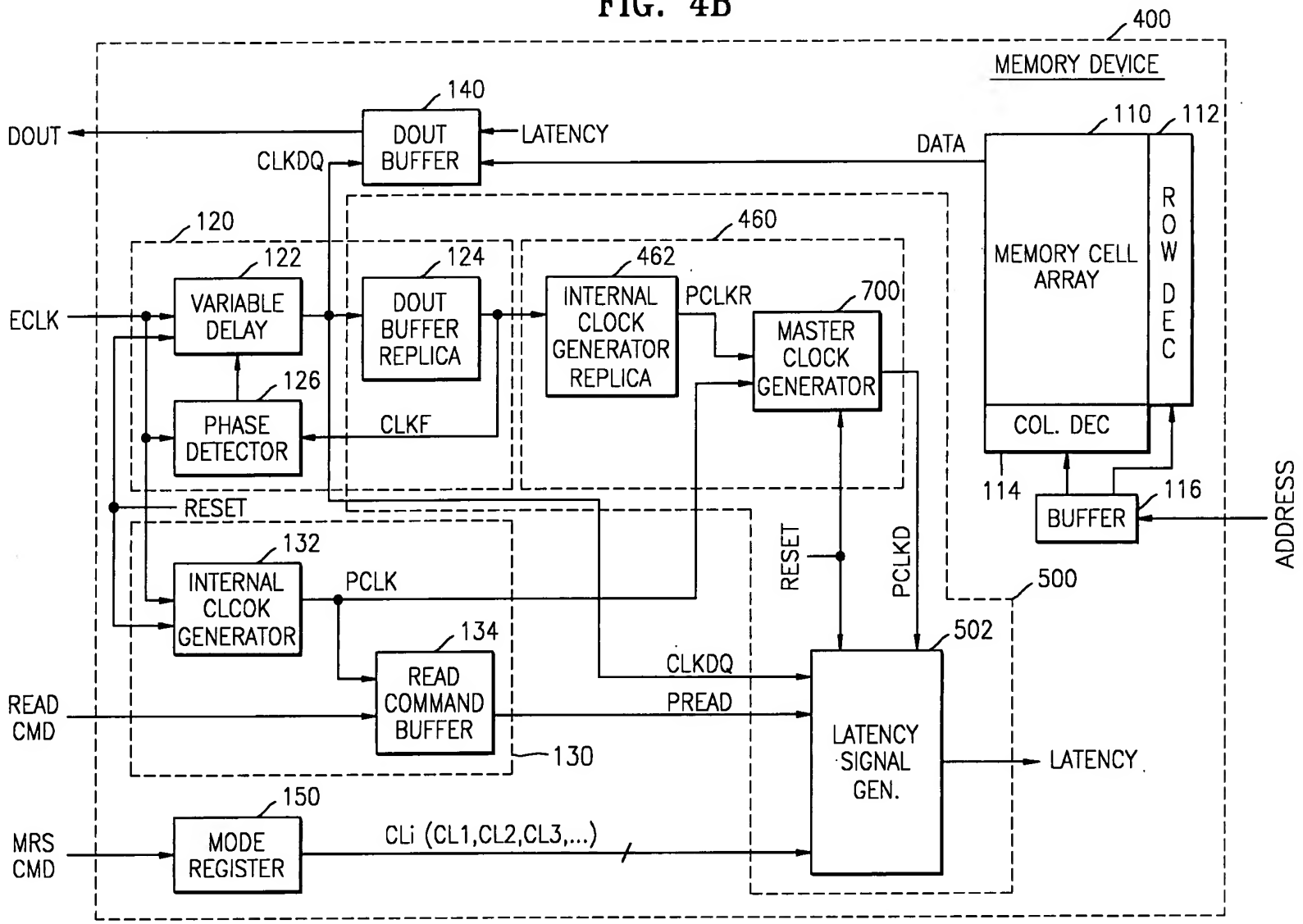

400
MEMORY DEVICE
140
DOUT BUFFER
DOUT
LATENCY
CLKDQ
DATA
110
112
MEMORY CELL ARRAY
ROW DEC
120
460
122
VARIABLE DELAY
124
DOUT BUFFER REPLICA
462
INTERNAL CLOCK GENERATOR REPLICA
PCLKR
700
MASTER CLOCK GENERATOR
ECLK
126
PHASE DETECTOR
CLKF
COL. DEC
114
116
BUFFER
ADDRESS
RESET
132
INTERNAL CLCOK GENERATOR
PCLK
RESET
PCLKD
500
502
134
READ COMMAND BUFFER
CLKDQ
READ CMD
PREAD
LATENCY SIGNAL GEN.
LATENCY
130
150
MODE REGISTER
MRS CMD
CLi (CL1,CL2,CL3,...)

FIG. 4C

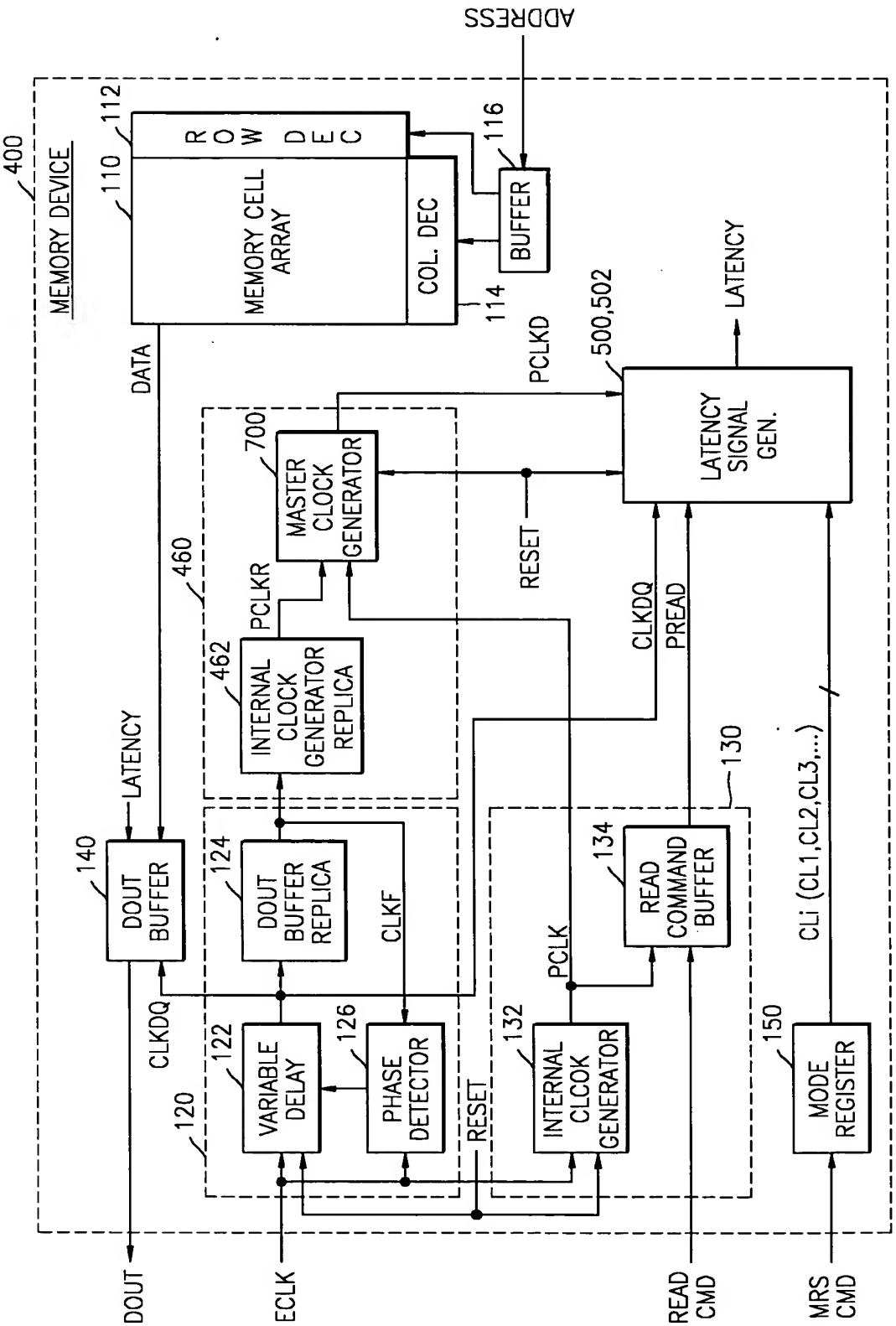

400
MEMORY DEVICE
110
MEMORY CELL ARRAY
112
ROW DEC
114
COL. DEC
116
BUFFER
ADDRESS
DATA
PCLKD
500,502
LATENCY
LATENCY SIGNAL GEN.
700
MASTER CLOCK GENERATOR
RESET
460
PCLKR
462
INTERNAL CLOCK GENERATOR REPLICA
CLKDQ
PREAD
130
LATENCY
140
DOUT BUFFER
124
DOUT BUFFER REPLICA
CLKF
134
READ COMMAND BUFFER
CLi (CL1,CL2,CL3,...)
PCLK
122
VARIABLE DELAY
126
PHASE DETECTOR
132
INTERNAL CLCOK GENERATOR
150
MODE REGISTER
120
RESET
DOUT
ECLK
READ CMD
MRS CMD

FIG. 5

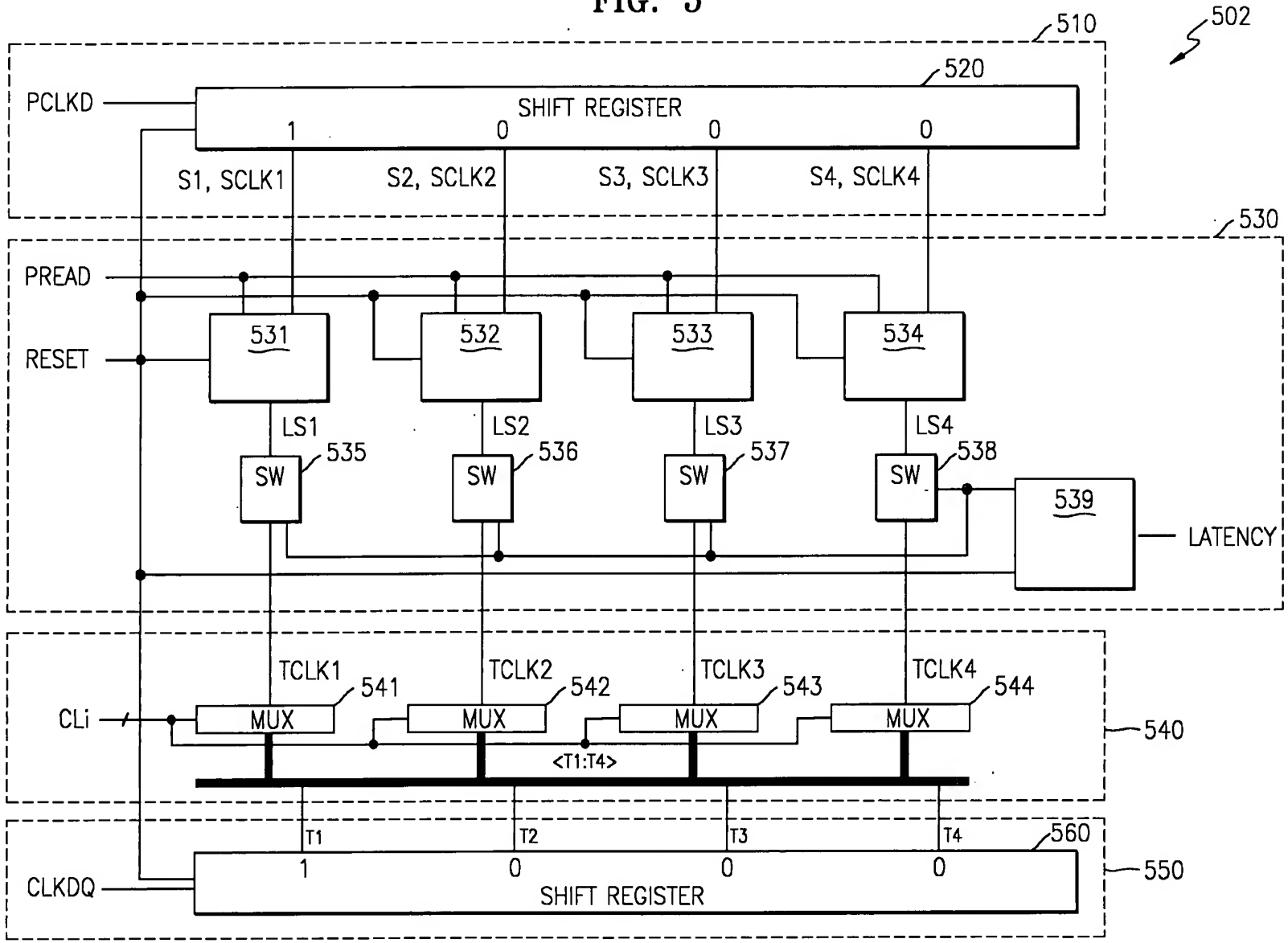

502
510
520
PCLKD
SHIFT REGISTER
1
0
0
0
S1, SCLK1
S2, SCLK2
S3, SCLK3
S4, SCLK4
530
PREAD
RESET
531
532
533
534
LS1
LS2
LS3
LS4
SW
535
536
537
538
539
LATENCY
TCLK1
TCLK2
TCLK3
TCLK4
CLi
MUX
541
542
543
544
540
<T1:T4>
T1
T2
T3
T4
560
CLKDQ
SHIFT REGISTER
550

FIG. 6

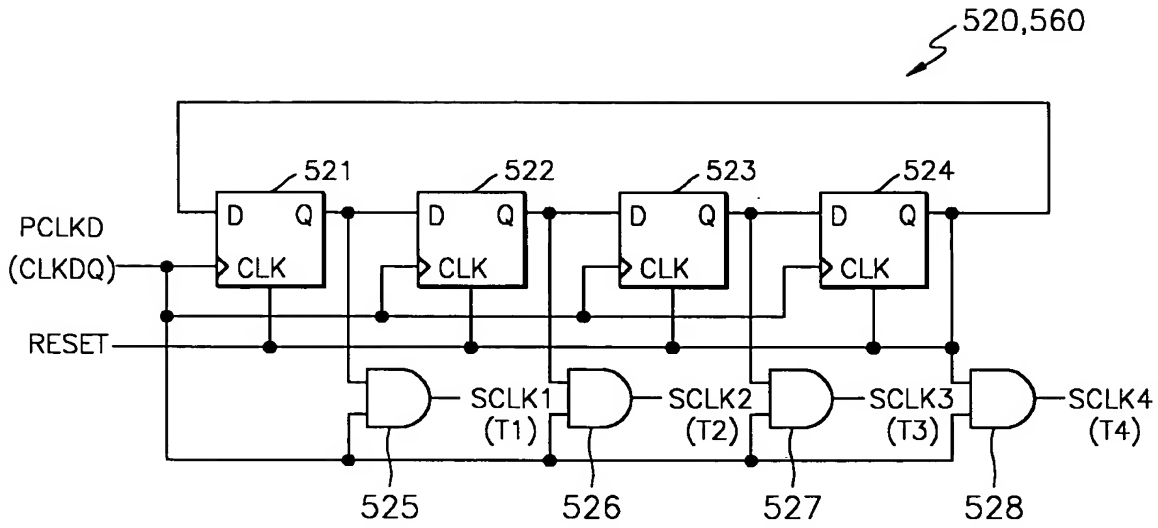

520,560
521
522
523
524
D
Q
CLK
PCLKD
(CLKDQ)
RESET
SCLK1
(T1)
SCLK2
(T2)
SCLK3
(T3)
SCLK4
(T4)
525
526
527
528

FIG. 7

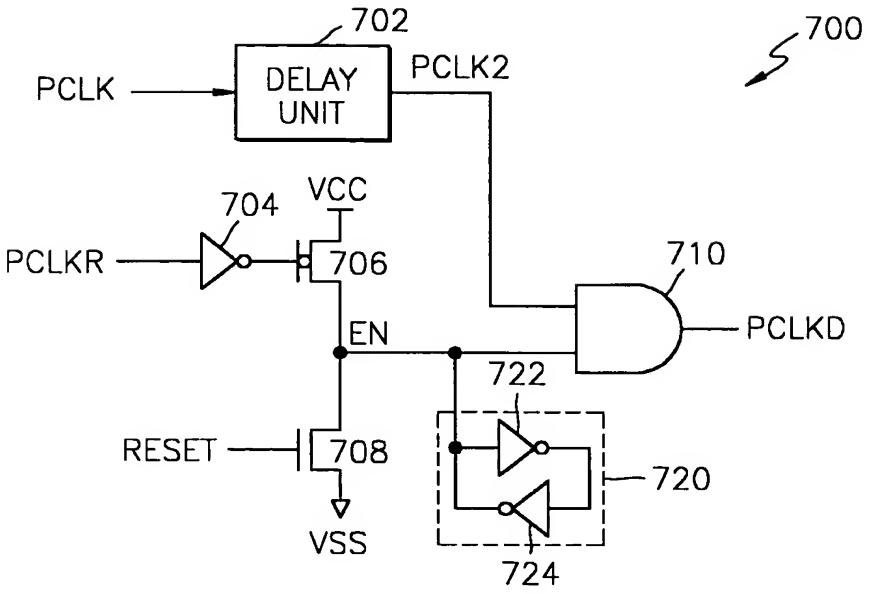
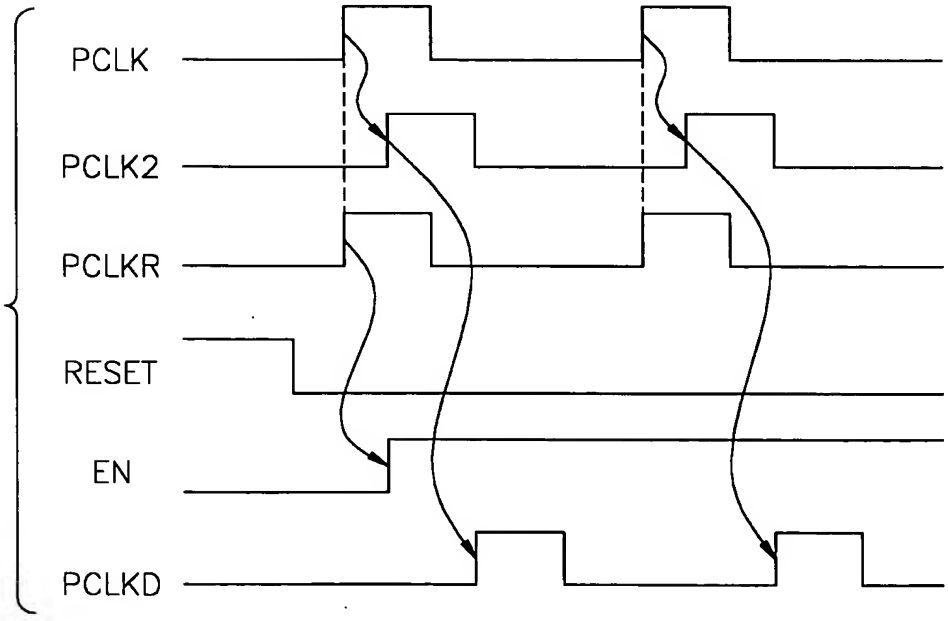

700
702
PCLK
DELAY UNIT
PCLK2
704
VCC
PCLKR
706
710
EN
PCLKD
722
RESET
708
720
VSS
724

FIG. 8


PCLK
PCLK2
PCLKR
RESET
EN
PCLKD

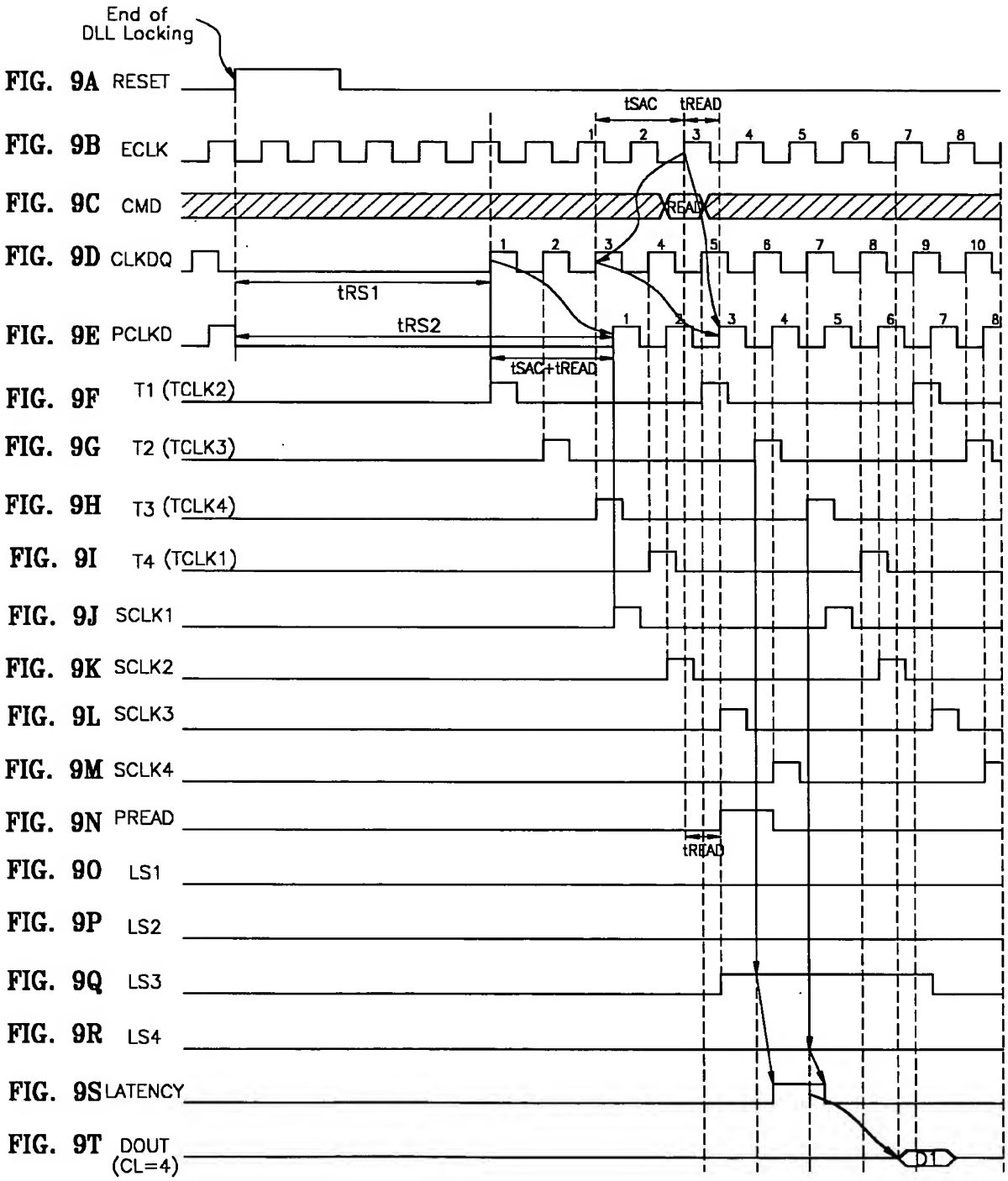

End of
DLL Locking
FIG. 9A RESET
tSAC
tREAD
FIG. 9B ECLK
1
2
3
4
5
6
7
8
FIG. 9C CMD
READ
FIG. 9D CLKDQ
1
2
3
4
5
6
7
8
9
10
tRS1
tRS2
FIG. 9E PCLKD
1
2
3
4
5
6
7
8
tSAC+tREAD
FIG. 9F T1 (TCLK2)
FIG. 9G T2 (TCLK3)
FIG. 9H T3 (TCLK4)
FIG. 9I T4 (TCLK1)
FIG. 9J SCLK1
FIG. 9K SCLK2
FIG. 9L SCLK3
FIG. 9M SCLK4
FIG. 9N PREAD
tREAD
FIG. 9O LS1
FIG. 9P LS2
FIG. 9Q LS3
FIG. 9R LS4
FIG. 9S LATENCY
FIG. 9T DOUT
(CL=4)
D1

FIG. 10A

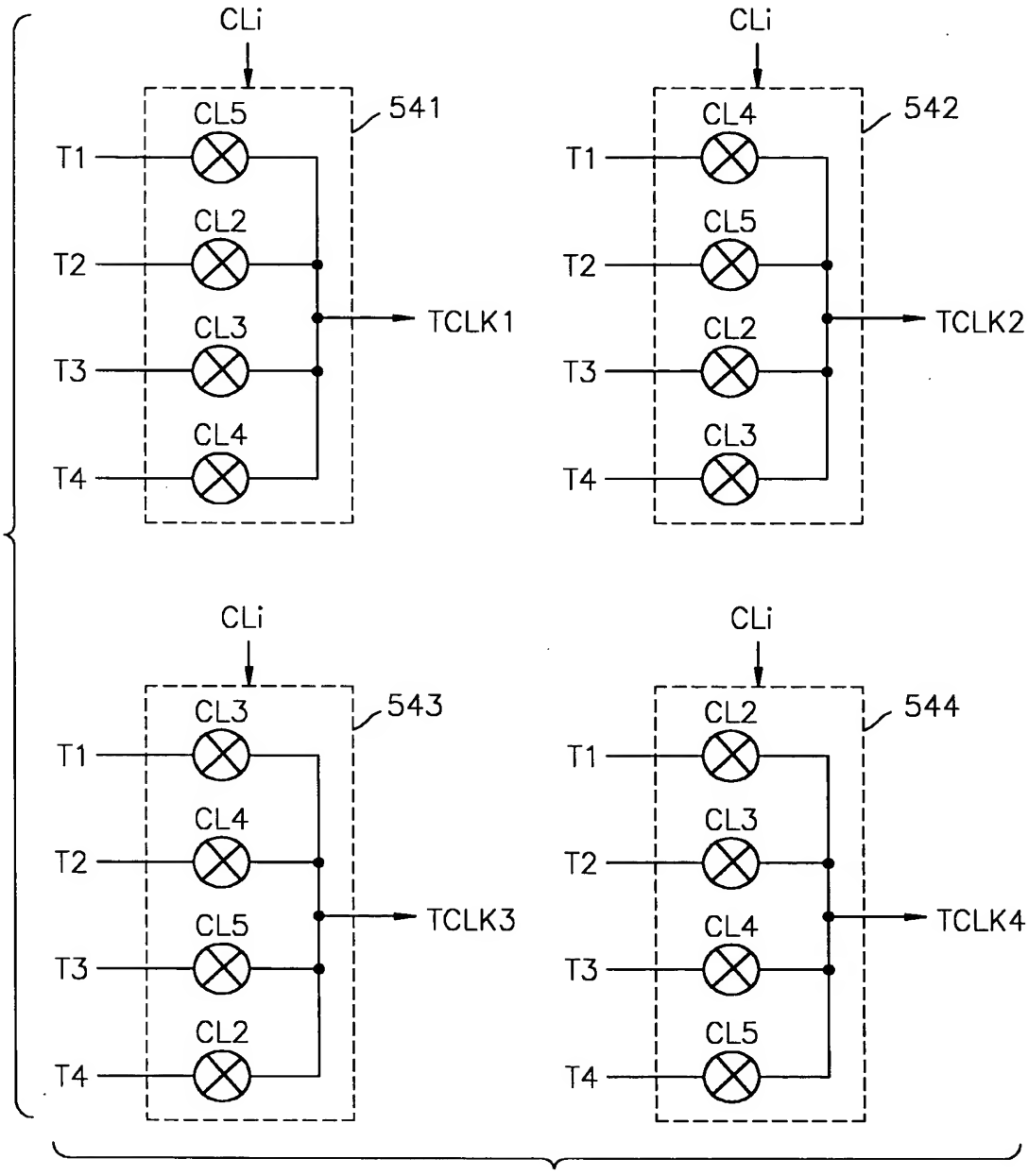
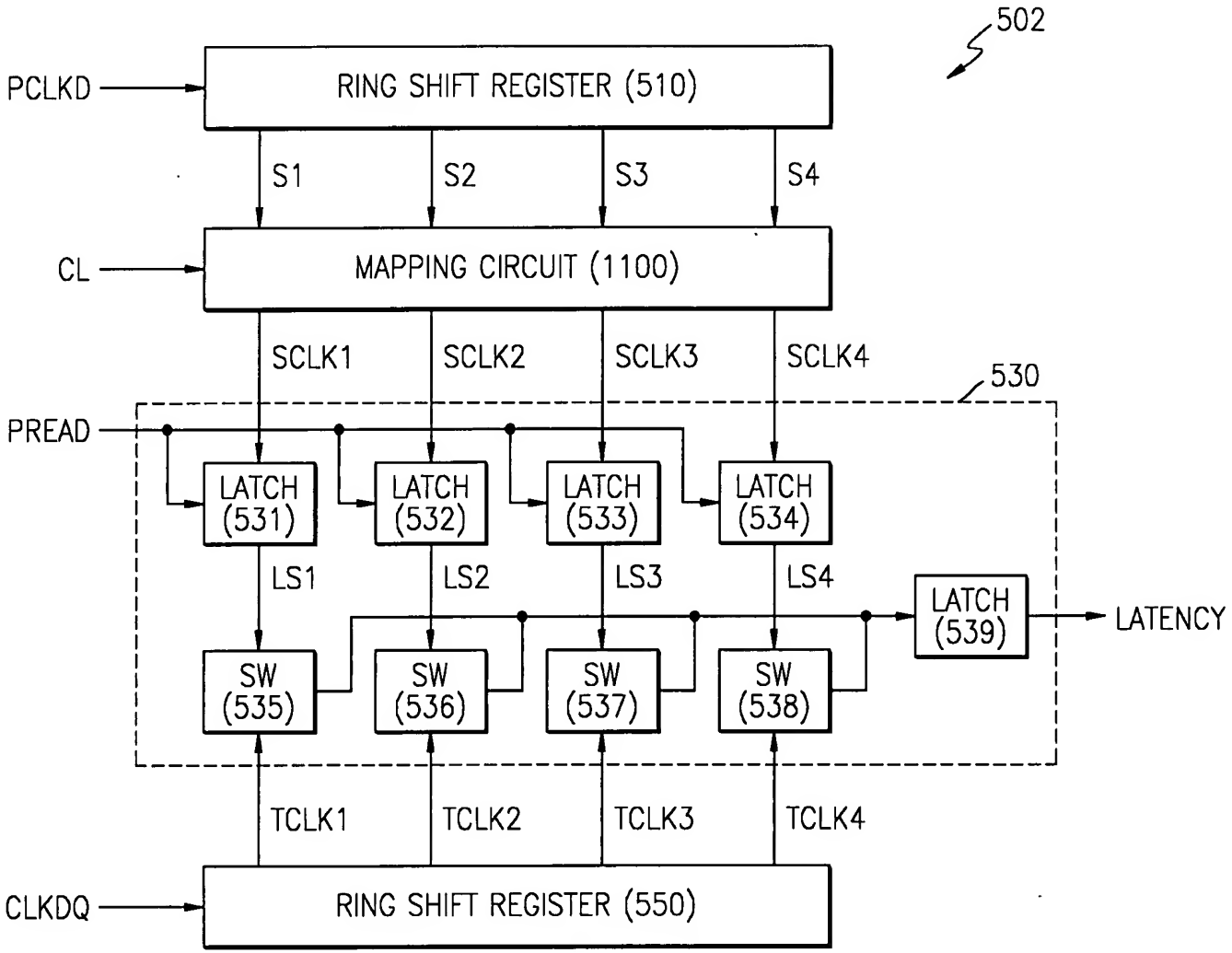

CLi
CL5
541
T1
CL2
T2
CL3
T3
CL4
T4
TCLK1
CLi
CL4
542
T1
CL5
T2
CL2
T3
CL3
T4
TCLK2
CLi
CL3
543
T1
CL4
T2
CL5
T3
CL2
T4
TCLK3
CLi
CL2
544
T1
CL3
T2
CL4
T3
CL5
T4
TCLK4

FIG. 10B

CL MODE	TCLK1	TCLK2	TCLK3	TCLK4
4	T4	T1	T2	T3
5	T1	T2	T3	T4
2	T2	T3	T4	T1
3	T3	T4	T1	T2

FIG. 11


502
PCLKD
RING SHIFT REGISTER (510)
S1
S2
S3
S4
CL
MAPPING CIRCUIT (1100)
SCLK1
SCLK2
SCLK3
SCLK4
530
PREAD
LATCH (531)
LATCH (532)
LATCH (533)
LATCH (534)
LS1
LS2
LS3
LS4
LATCH (539)
LATENCY
SW (535)
SW (536)
SW (537)
SW (538)
TCLK1
TCLK2
TCLK3
TCLK4
CLKDQ
RING SHIFT REGISTER (550)

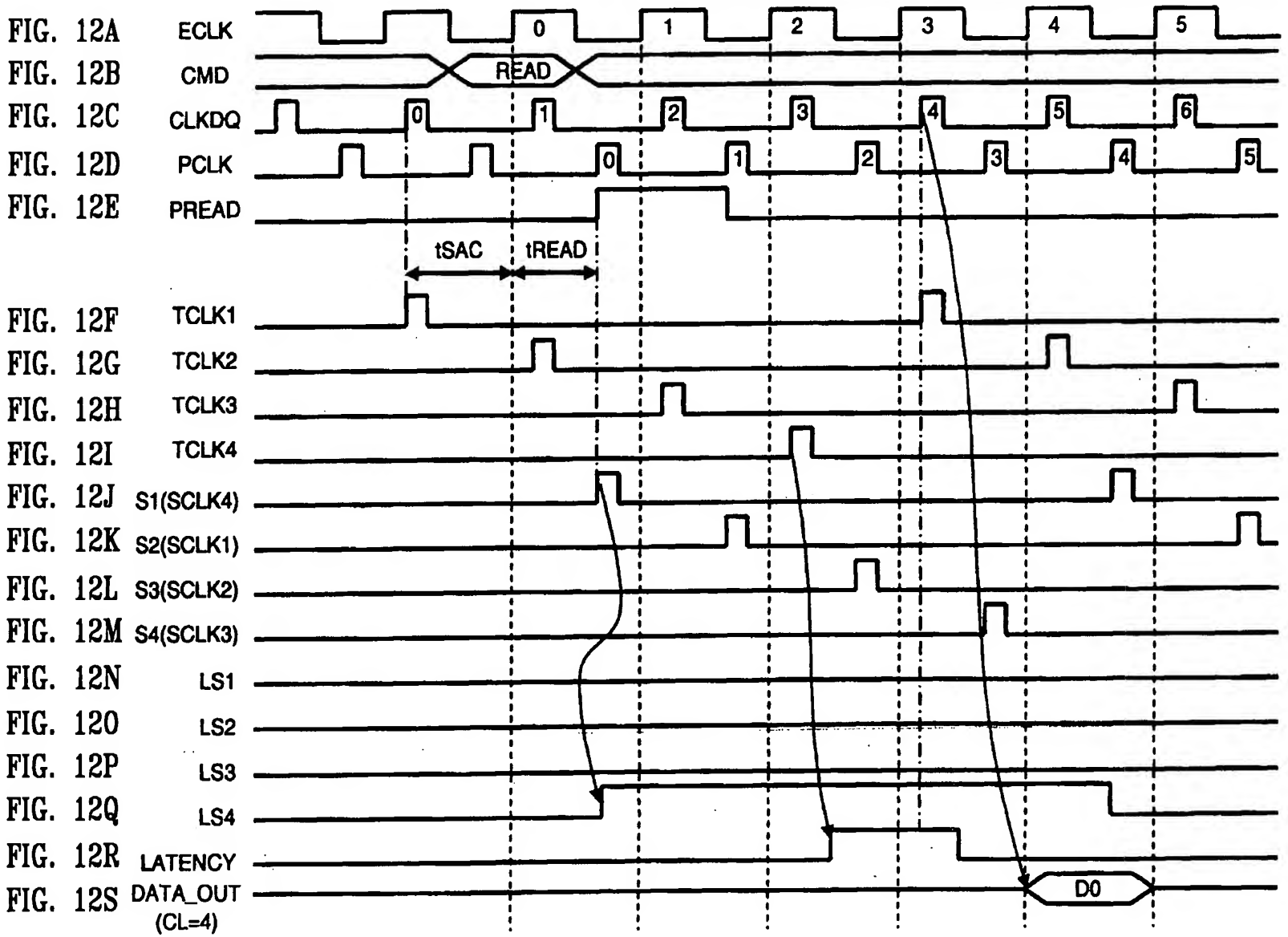


FIG. 12A
ECLK
0
1
2
3
4
5
FIG. 12B
CMD
READ
FIG. 12C
CLKDQ
0
1
2
3
4
5
6
FIG. 12D
PCLK
0
1
2
3
4
5
FIG. 12E
PREAD
tSAC
tREAD
FIG. 12F
TCLK1
FIG. 12G
TCLK2
FIG. 12H
TCLK3
FIG. 12I
TCLK4
FIG. 12J
S1(SCLK4)
FIG. 12K
S2(SCLK1)
FIG. 12L
S3(SCLK2)
FIG. 12M
S4(SCLK3)
FIG. 12N
LS1
FIG. 12O
LS2
FIG. 12P
LS3
FIG. 12Q
LS4
FIG. 12R
LATENCY
FIG. 12S
DATA_OUT
(CL=4)
D0

FIG. 13A

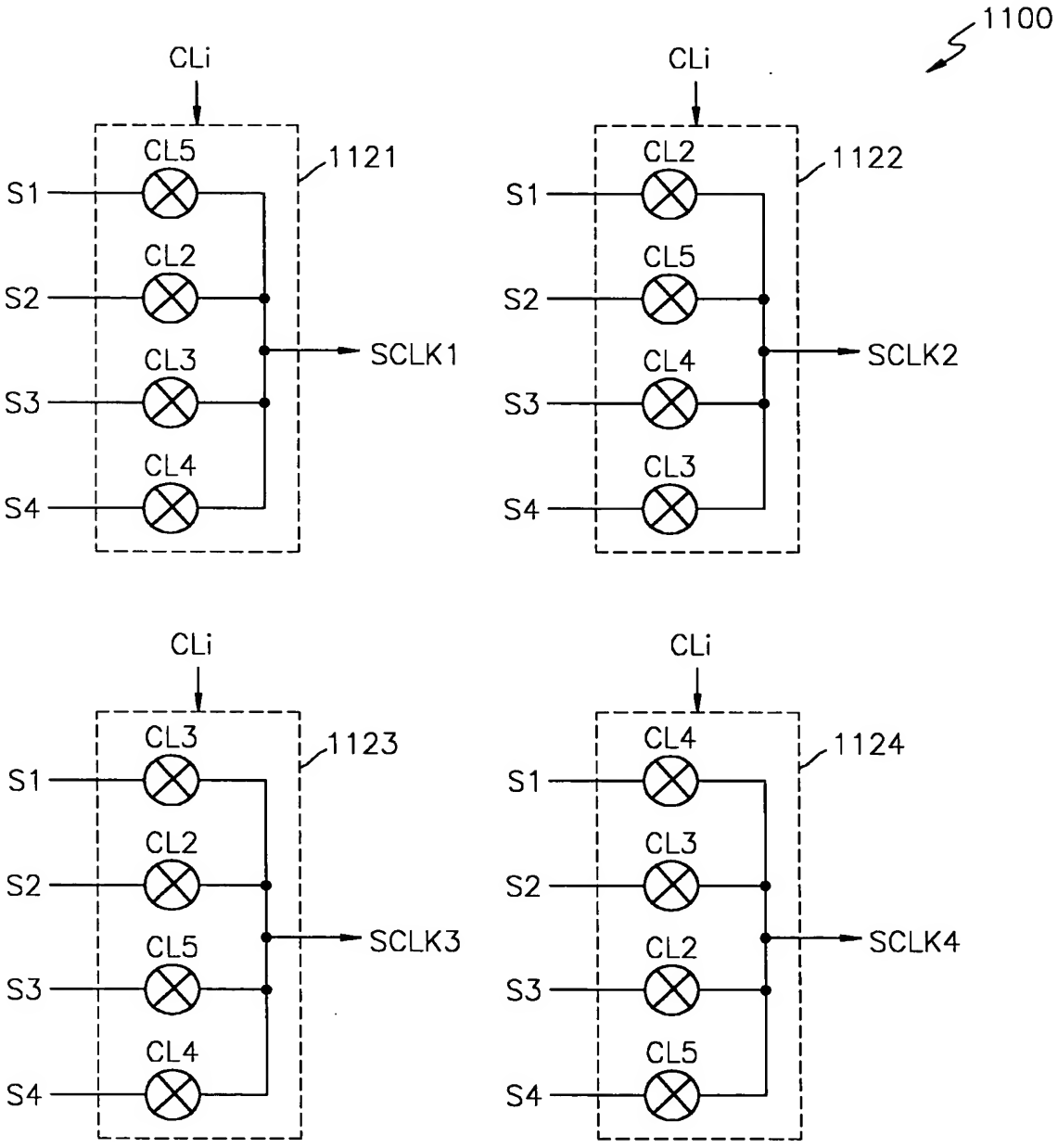

1100
CLi
CL5
1121
S1
CL2
S2
CL3
S3
CL4
S4
SCLK1
CLi
CL2
1122
S1
CL5
S2
CL4
S3
CL3
S4
SCLK2
CLi
CL3
1123
S1
CL2
S2
CL5
S3
CL4
S4
SCLK3
CLi
CL4
1124
S1
CL3
S2
CL2
S3
CL5
S4
SCLK4

FIG. 13B

CL	SCLK1	SCLK2	SCLK3	SCLK4
2	S4	S1	S2	S3
3	S3	S4	S1	S2
4	S2	S3	S4	S1
5	S1	S2	S3	S4

FIG. 14

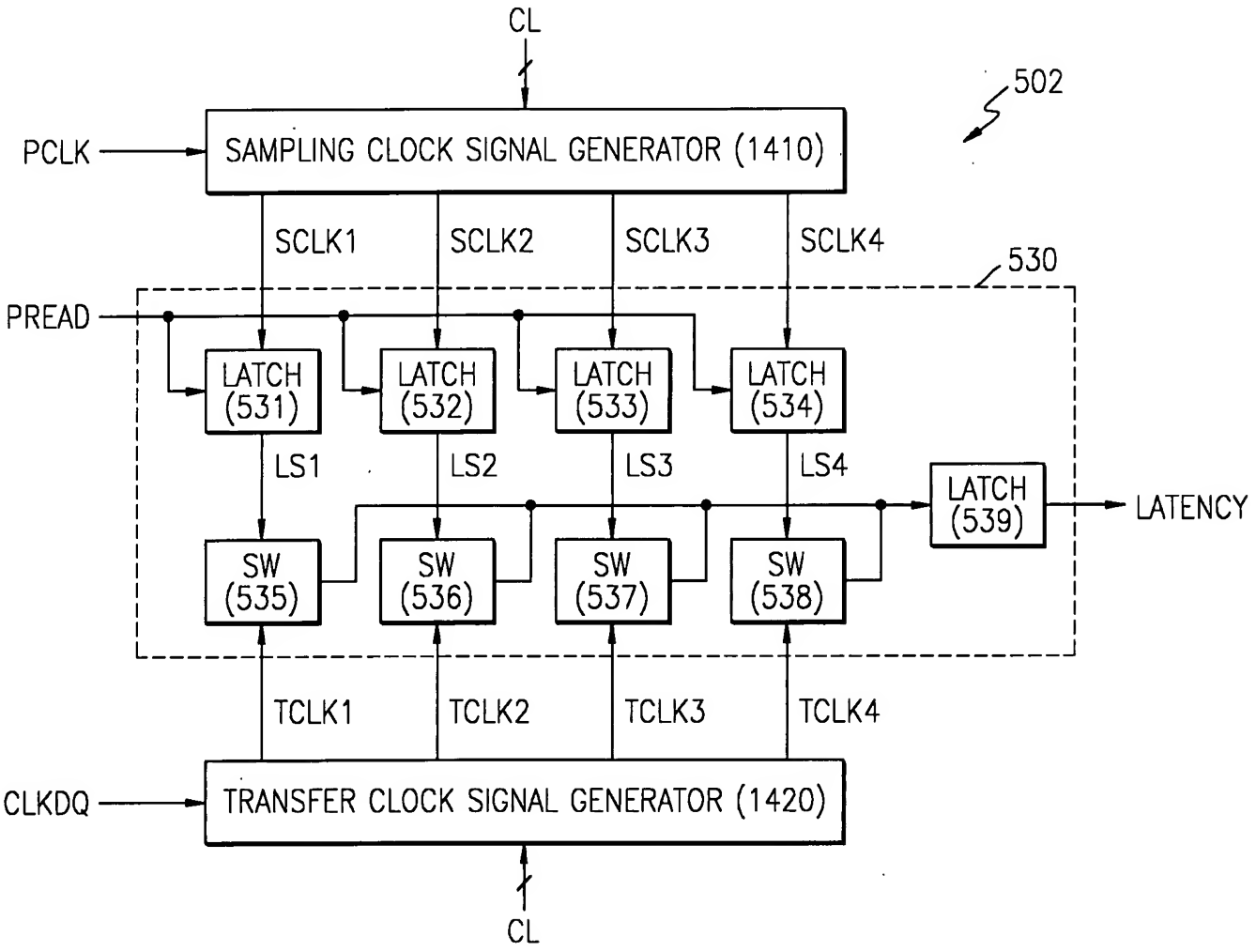

CL
502
PCLK
SAMPLING CLOCK SIGNAL GENERATOR (1410)
SCLK1
SCLK2
SCLK3
SCLK4
530
PREAD
LATCH (531)
LATCH (532)
LATCH (533)
LATCH (534)
LS1
LS2
LS3
LS4
LATCH (539)
LATENCY
SW (535)
SW (536)
SW (537)
SW (538)
TCLK1
TCLK2
TCLK3
TCLK4
CLKDQ
TRANSFER CLOCK SIGNAL GENERATOR (1420)
CL

FIG. 15

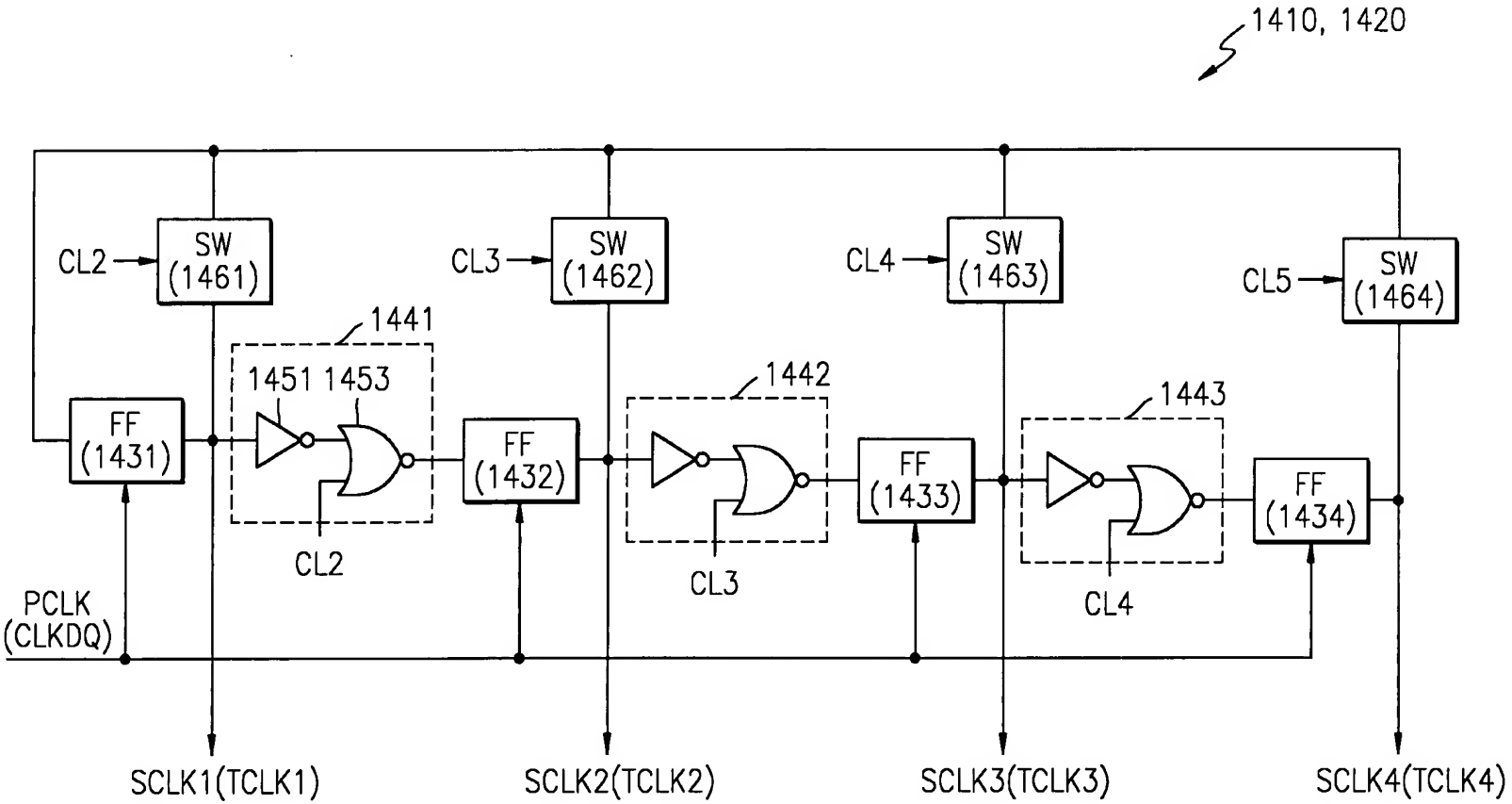

1410, 1420
CL2
SW (1461)
CL3
SW (1462)
CL4
SW (1463)
CL5
SW (1464)
1441
1451 1453
1442
1443
FF (1431)
FF (1432)
FF (1433)
FF (1434)
CL2
CL3
CL4
PCLK (CLKDQ)
SCLK1(TCLK1)
SCLK2(TCLK2)
SCLK3(TCLK3)
SCLK4(TCLK4)

FIG. 16

CL2								
TCLK1	0		1	1	1	1	1	1
TCLK2	0		0	0	0	0	0	0
TCLK3	0		0	0	0	0	0	0
TCLK4	0		0	0	0	0	0	0

CL4								
TCLK1	0		1	0	0	1	0	0
TCLK2	0		0	1	0	0	1	0
TCLK3	0		0	0	1	0	0	1
TCLK4	0		0	0	0	0	0	0

CL3								
TCLK1	0		1	0	1	0	1	0
TCLK2	0		0	1	0	1	0	1
TCLK3	0		0	0	0	0	0	0
TCLK4	0		0	0	0	0	0	0

CL5								
TCLK1	0		1	0	0	0	1	0
TCLK2	0		0	1	0	0	0	1
TCLK3	0		0	0	1	0	0	0
TCLK4	0		0	0	0	1	0	0

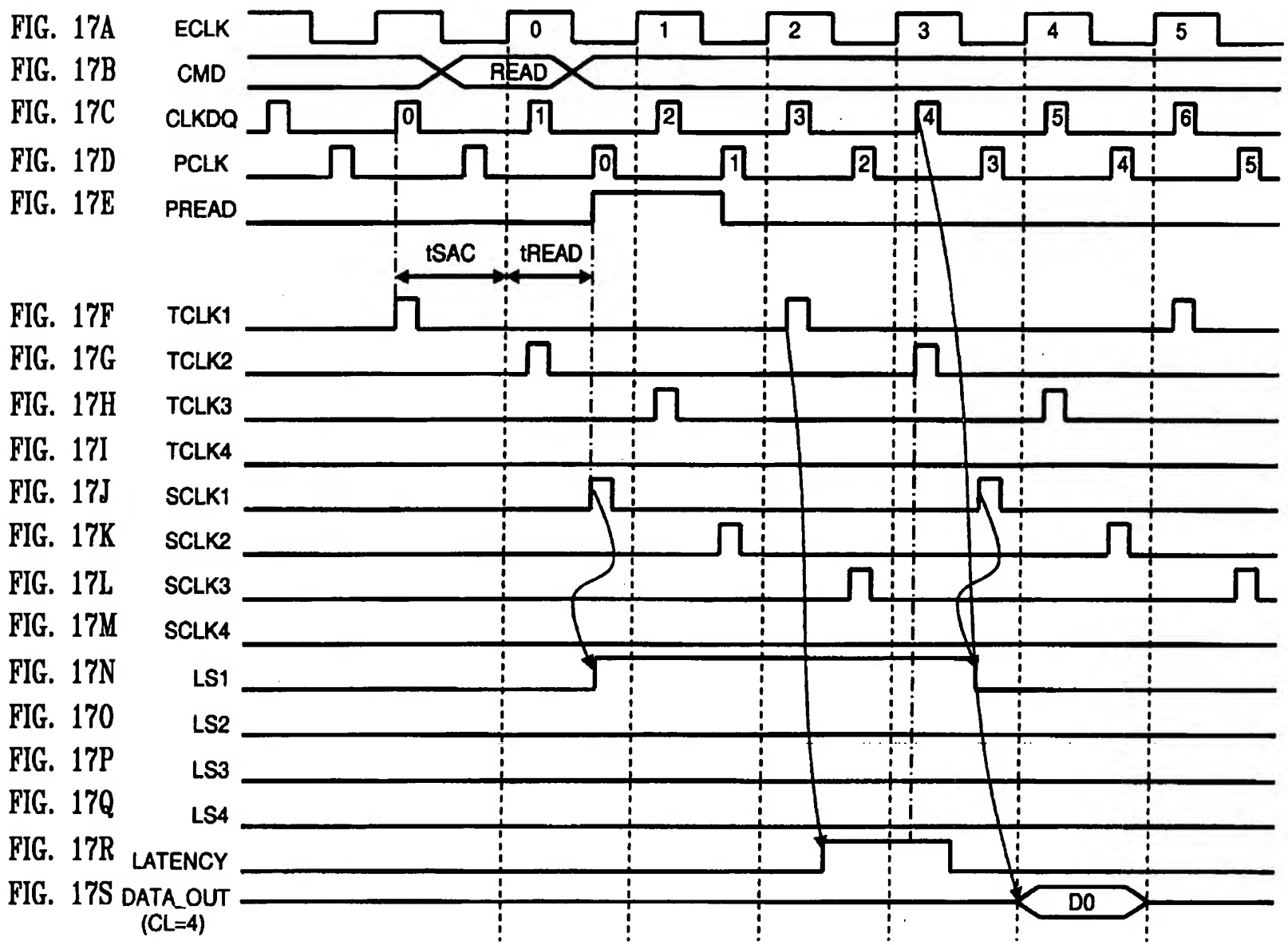


FIG. 17A
ECLK
0
1
2
3
4
5
FIG. 17B
CMD
READ
FIG. 17C
CLKDQ
0
1
2
3
4
5
6
FIG. 17D
PCLK
0
1
2
3
4
5
FIG. 17E
PREAD
tSAC
tREAD
FIG. 17F
TCLK1
FIG. 17G
TCLK2
FIG. 17H
TCLK3
FIG. 17I
TCLK4
FIG. 17J
SCLK1
FIG. 17K
SCLK2
FIG. 17L
SCLK3
FIG. 17M
SCLK4
FIG. 17N
LS1
FIG. 17O
LS2
FIG. 17P
LS3
FIG. 17Q
LS4
FIG. 17R
LATENCY
FIG. 17S
DATA_OUT
(CL=4)
D0

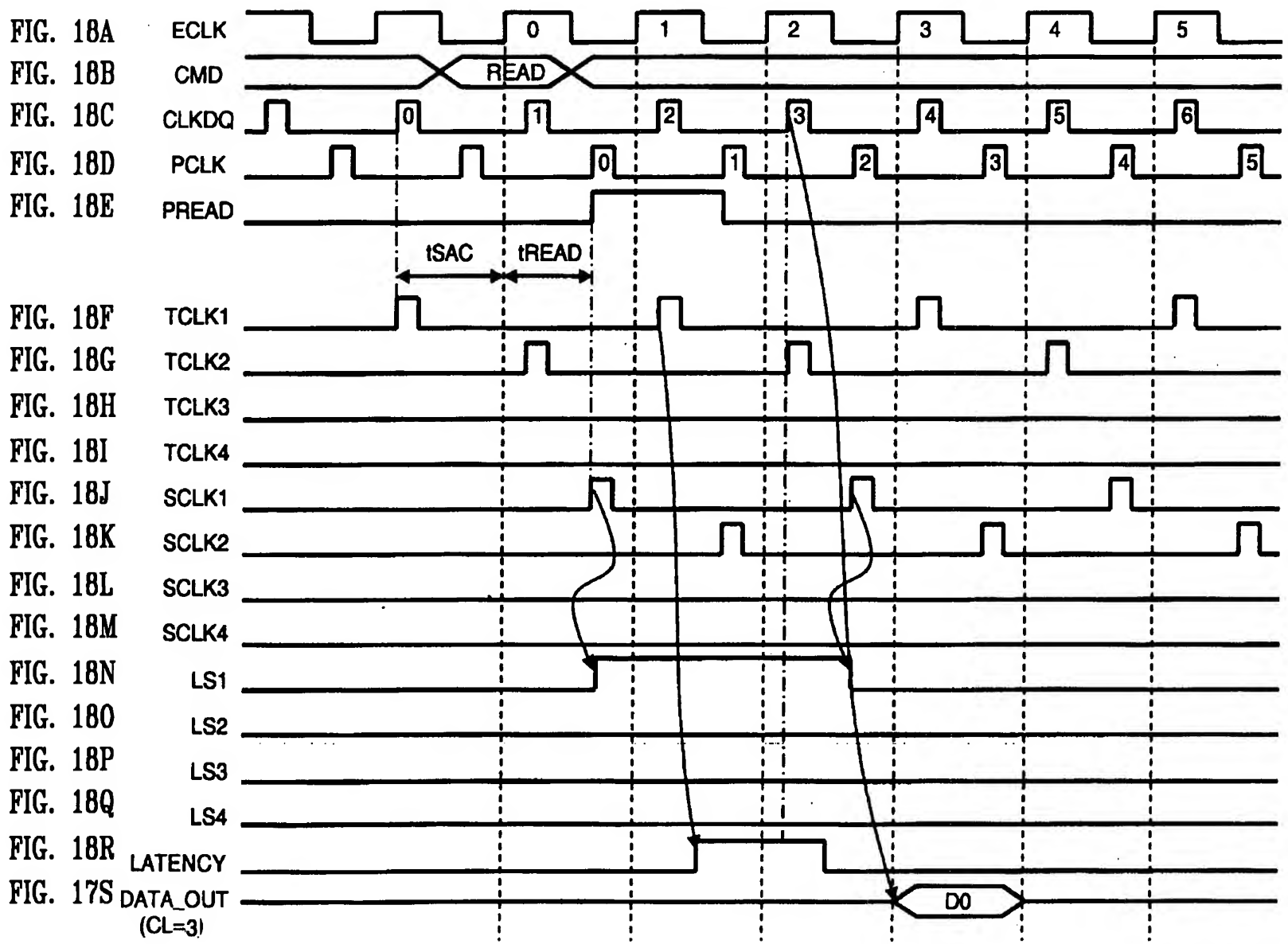


FIG. 18A
ECLK
0
1
2
3
4
5
FIG. 18B
CMD
READ
FIG. 18C
CLKDQ
0
1
2
3
4
5
6
FIG. 18D
PCLK
0
1
2
3
4
5
FIG. 18E
PREAD
tSAC
tREAD
FIG. 18F
TCLK1
FIG. 18G
TCLK2
FIG. 18H
TCLK3
FIG. 18I
TCLK4
FIG. 18J
SCLK1
FIG. 18K
SCLK2
FIG. 18L
SCLK3
FIG. 18M
SCLK4
FIG. 18N
LS1
FIG. 18O
LS2
FIG. 18P
LS3
FIG. 18Q
LS4
FIG. 18R
LATENCY
FIG. 17S
DATA_OUT
(CL=3)
D0

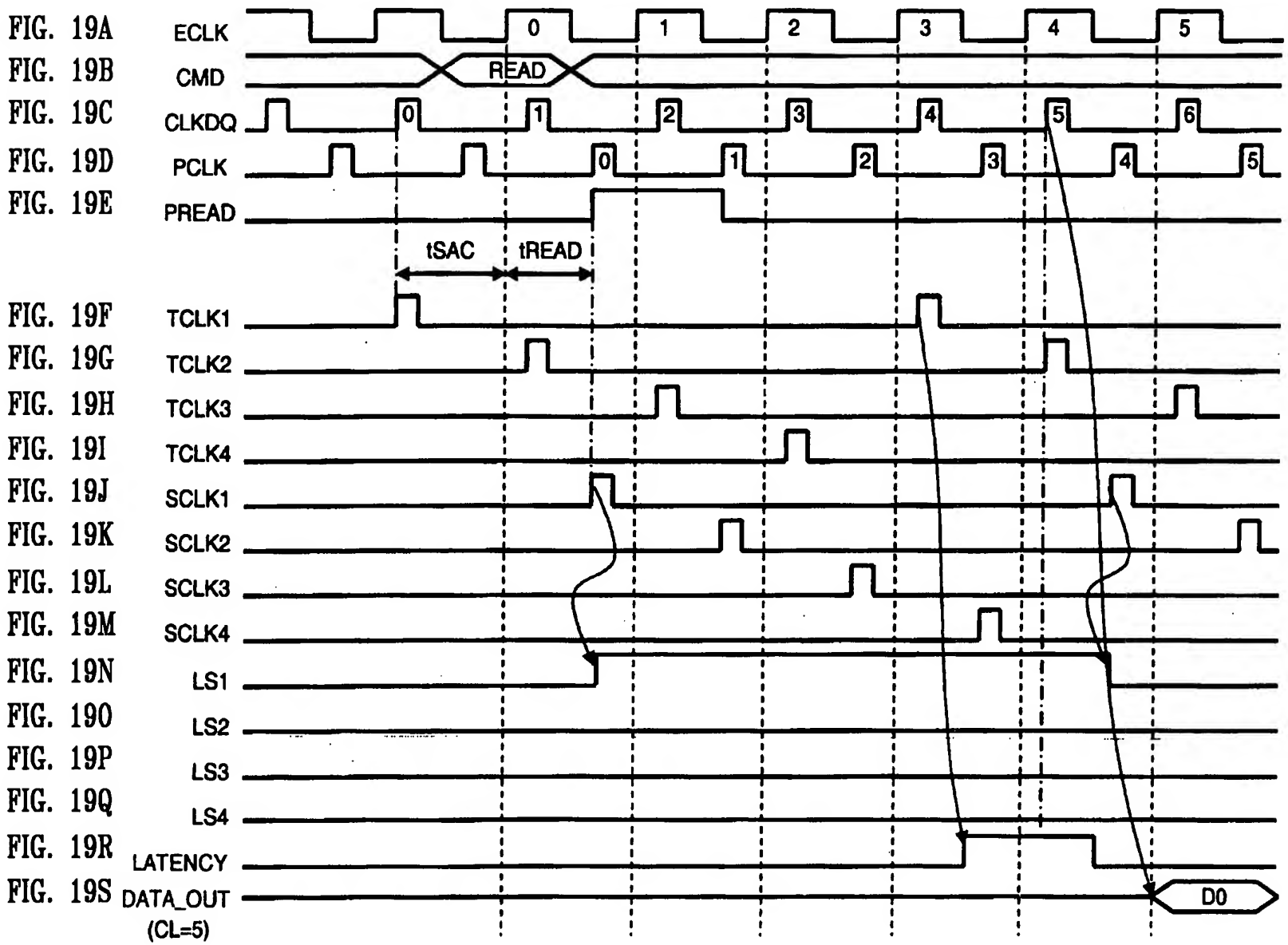


FIG. 19A
FIG. 19B
FIG. 19C
FIG. 19D
FIG. 19E
FIG. 19F
FIG. 19G
FIG. 19H
FIG. 19I
FIG. 19J
FIG. 19K
FIG. 19L
FIG. 19M
FIG. 19N
FIG. 19O
FIG. 19P
FIG. 19Q
FIG. 19R
FIG. 19S
ECLK
CMD
CLKDQ
PCLK
PREAD
tSAC
tREAD
TCLK1
TCLK2
TCLK3
TCLK4
SCLK1
SCLK2
SCLK3
SCLK4
LS1
LS2
LS3
LS4
LATENCY
DATA_OUT
(CL=5)
READ
0
1
2
3
4
5
6
D0